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ORIGINAL ARTICLE

Enhancing Photoresponse by Synergy of Electric Double Layer Gate and Illumination in Single CuTCNQ NW Field Effect Transistors

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Abstract: We report that photoresponse of a single metal-organic charge transfer complex Cu: TCNQ nanowire (NW) can be enhanced simultaneously by illumination as well as applying a gate bias in an Electric Double Layer Field Effect Transistor (EDL-FET) configuration fabricated on Cu: TCNQ as a channel. It is observed that applying a bias using an EDL gate to a n-channel Cu: TCNQ single NW FET, one can enhance the photoresponse of the Cu: TCNQ substantially over that which arise from the photoconductive response alone. Electron-hole pairs that generate in the NW under illuminated of wavelength 400 nm gives rise photo current. Also, electric double layer induce negative charges in the NW channel which effectively increases the carrier concentration, contributing to better response in conduction. The effect reported here has a generic nature that gives rise to a class of gated photodetectors of different photoresponsive materials.

Keywords: Cu: TCNQ nanowire; EDL FET; photoresponse

1. Introduction

Over the last decade, there has been growing interest in room temperature ionic liquids and their potential application as dielectric gate to control physical properties of different functional materials becomes an active field of research[1]. Ionic liquid now have attracted much attention due to their wide electrochemical windows, low vapor pressures, and high chemical and physical stability. A mixture of polyethylene oxide (PEO) and the solid electrolyte LiClO4 is a commonly used material as ionic liquid[2]. Other way, copper-tetracyanoquinodimethane (Cu: TCNQ), a metal-organic charge transfer complex is well known photoconductive materials[3] and its electrical conductivity can be tuned by external perturbation like electric field[4], reduced graphitic oxide[5] etc. In this report, I have demonstrated that a synergy between an applied gate bias and illumination can lead to a substantial enhancement of photocurrent in Cu: TCNQ NW when it is used as a channel in an electric double layer field effect transistor (EDL-FET) configuration.

2. Materials and Methods

2.1 Growth of Cu: TCNQ NWs

The single NW devices is fabricated from Cu: TCNQ NWs grown by vapour phase deposition of deposition of TCNQ on to a heated Cu-film (kept at ~130 °C) grown on a glass substrate. The charge transfer reaction of TCNQ with Cu leads to formation of Cu: TCNQ and growth of NW that involves diffusion of Cu through the growing Cu:TCNQ NW.

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The Cu that diffuses along the length of the NW acts as a fresh supply source for further reaction and growth. Fourier Transform Infra-red (FTIR) spectroscopic measurement confirms the formation of Cu:TCNQ and used to establish the extent of charge transfer in Cu: TCNQ from Cu to TCNQ[5]. NWs grown from vapour phase are tetragonal in crystal structure as characterized by X-Ray Diffraction (XRD) and Transmission Electron Microscope (TEM)[4].

2.2 Fabrication of EDL-FET single NW device

NWs grown from vapour phase are separated from the glass substrate by ultrasonication with ethanol as base liquid. Ultrasonicated NWs are then dispersed on 300 nmSiO2/Si substrate containing predefined electrodes of few tens of nanometer spacing. Identifying an isolated single NW with Scanning Electron Microscope (SEM), it is then connected with Focused Electron Beam (FIB) deposited Pt. Two outer electrodes connecting the NWs act as source (S) and drain (D). A 10:1 mixture of poly (ethylene oxide) (PEO) and Lithium perchlorate (LiClO4) is used as a gate dielectric.. Microdrop of PEO/LiClO4 is placed in between S and D and used as gate dielectric material. A thin Cu wire is used to apply the bias to the electrolyte. The electrolyte at the interface with Cu: TCNQ forms an electric double layer (EDL). Schematic of EDL-FET is illustrated in Figure 1(A). Figure 1(B) represents the SEM image of the Cu: TCNQ NW connected with FIB deposited Pt.

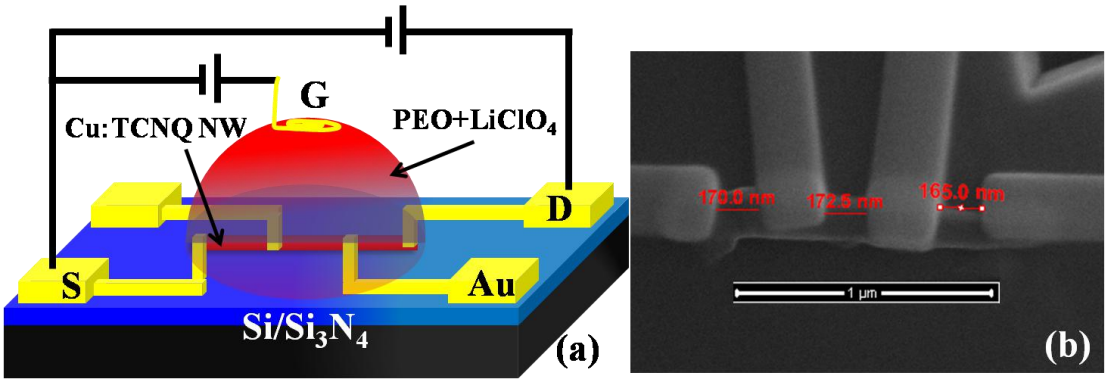

Figure 1: (A) Schematic representation of electric double layer FET with PEO + LiClO4 ionic liquid as a dielectric medium. (B) Cu: TCNQ single nanowire connected with four FIB deposited Pt electrode used as a channel material

The measurements were performed in ambient atmosphere. Output and transconductance characteristics of the device are measured using Keitheley SM-4210, where voltage is the source and current is the measured quantity. Constant gate bias in control gate is applied from another sourcemeter source and corresponding gate-current was measured with the same to ensure that the gate current remains a small fraction of the drain current.

3. Ethics Statement

As an author, I certify that

1. This material has not been published in whole or in part elsewhere
2. The manuscript is not currently being considered for publication in another journal

4. Results and Discussion

The output characteristics i.e. drain current (I_{DS}) for the EDL-FET is measured as a function of drain-source voltage (V_{DS}) and measuring for different values of gate-source voltage (V_G). The quality of the FET was checked by measuring the gate current (I_G) for a given drain-source voltage. Figure 2(A) shows enhancement of I_{DS} (green line) for positive gate bias V_{DS} of 0.4 volt, which is almost 3 times higher (black line) compared to zero gate bias. Same measurement

has been performed under illumination of wavelength λ = 400 nm with gate dielectric on the same device. Combine effect of dielectric gate and illumination enhances the effect to ~4 times compare to that of dark current as shown in Figure 2. At all values of the V_{DS} used, gate current $I_G \leq 10^{-3} I_{DS}$, ensuring that the device operates as a FET. Gate current I_G as a function of V_{DS} is shown in Figure 2(B). Enhancement of current due to induced charge in the channel material by the gate dielectric is shown in Figure 2(C), whereas Figure 2(D) shows the important result that on illumination there is substantial photo-response when both gate and illumination are applied together. Comparative study of device current I_{DS} has been performed in Table 1 without and with gate bias applied to show the effect of illumination and applied bias individually. Application of gate bias of 0.4 volt enhances the device current almost 10 percent which is significantly large for such low bias. Thus, the application of the gate leads to substantial enhancement of the photoresponse of the device over that expected from photoconductive response alone

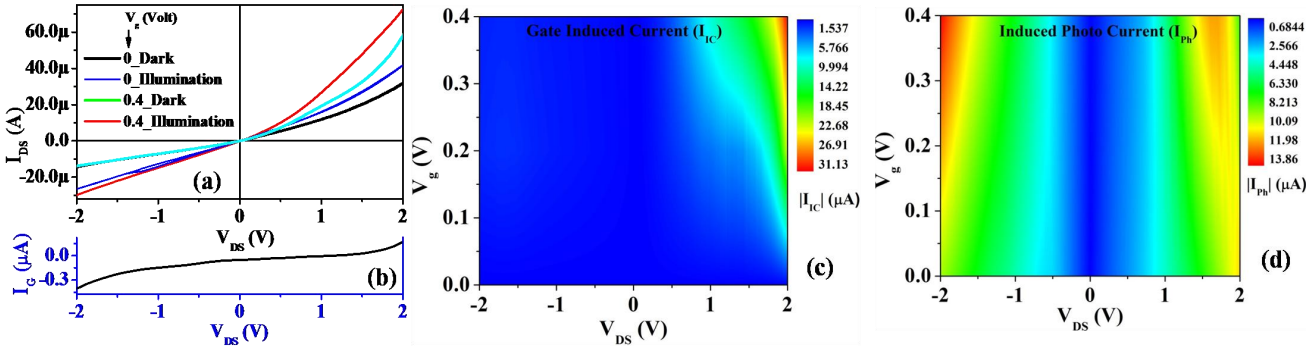

Figure 2: (A) Output characteristic of EDL-FET with of Cu: TCNQ single NW channel in dark and under 400nm illumination. (B) Gate current (Ig) of the same is ~ 103 times lower compared to device current (IDS) ensuring proper FET operation. (C) Induced dark current due to applied gate bias and (D) Induced photo current with applied gate bias.

Tables 1：Comparative study of I_{DS} with different V_g under dark and illumination

Vg (V)	IDS (illu)/IDS (dark)	Enhancement of IDS (%)
0	1.3	26
0.4	1.5	34

Fig. 2 Electric field distribution along the x-axis: the ellipse whose center is considered as the origin of x-y plane has minor and major axes of b and a respectively and is illuminated with a plane wave with $\varphi_0 = 180^\circ$ at 1 GHz frequency (λ denotes the wavelength in free space).

The synergy effect can be appreciated as described below. With zero gate bias the ratio of photo current to dark current $\left(\frac{I_{illu}}{I_{dark}}\right)$ is 1.3. Under an applied gate bias of V_g = 0.4 V when the FET is on, the ratio of photo current to dark current $\left(\frac{I_{illu}}{I_{dark}}\right)$ is 1.5. When the FET is illuminated with light, if the two carrier generation process simply add-up, then at V_g = 0.4 V, the expected current ration should be same without and with gate bias. Instead, enhancement observed is larger which indicated the synergy effect between gate and illumination.

Stability of the device current with time is also measured as shown in the Figure 3. It shows photocurrent

responses of the device on light illumination showing time-dependent photosensitivity with a time interval of 0.3 s at Vg = 0V and V_{DS} =1V. Experimental results demonstrate that there is no persistence in the photocurrent and device current is also stable with time.

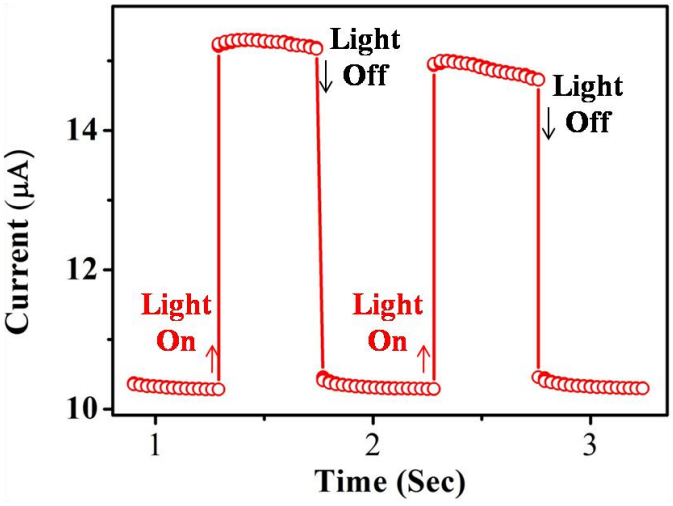

Figure 3: Constant bias device current as a function of time with illumination 'ON' and 'OFF'. Curve represents fast switching of device current with illumination and stable current with time. Data is for VDS = 1V and Vg = 0V.

To understand the mechanism and reason behind enhancement of current due to positive gate voltage of the NW FET, a process is schematically represented in Figure 4(A). This enhancement of current for positive gate bias is due to charge induced in the NW. When a gate voltage V_g is applied between the gate electrode and the source connected with the channel material (Cu: TCNQ), the electric field drives ions in the electrolyte toward both the channel and the gate electrode. Eventually, the ions stabilize just above the channel surface, forming a charged plane called the Helmholtz plane. The Helmholtz plane and the electrode surface are oppositely charged, forming a kind of capacitor called an electric double layer (EDL). Application of positive V_g induces negative charge in the channel material through the formation of ClO^{4-} near the gate electrode and K^{+} near the channel surface as illustrated in Figure 4(A). A gate-controlled metal-semiconductor barrier modulation is also proposed to interpret the carrier transport in Cu:TCNQ where charge is accumulated near in the channel due to bend bending by applied gate bias (Figure 4A(ii) and (iii)). Since Cu: TCNQ NW is an n-type semiconductor[6] *i.e.* majority carrier of conduction is electron, thus accumulated electrons on the channel surface by EDL increase the carrier concentration. This effectively enhances the electric current through the channel between the source and drain electrodes. Thus, the system works as a FET with an EDL gate capacitor of nanoscale thickness and can be described as EDL-FET.

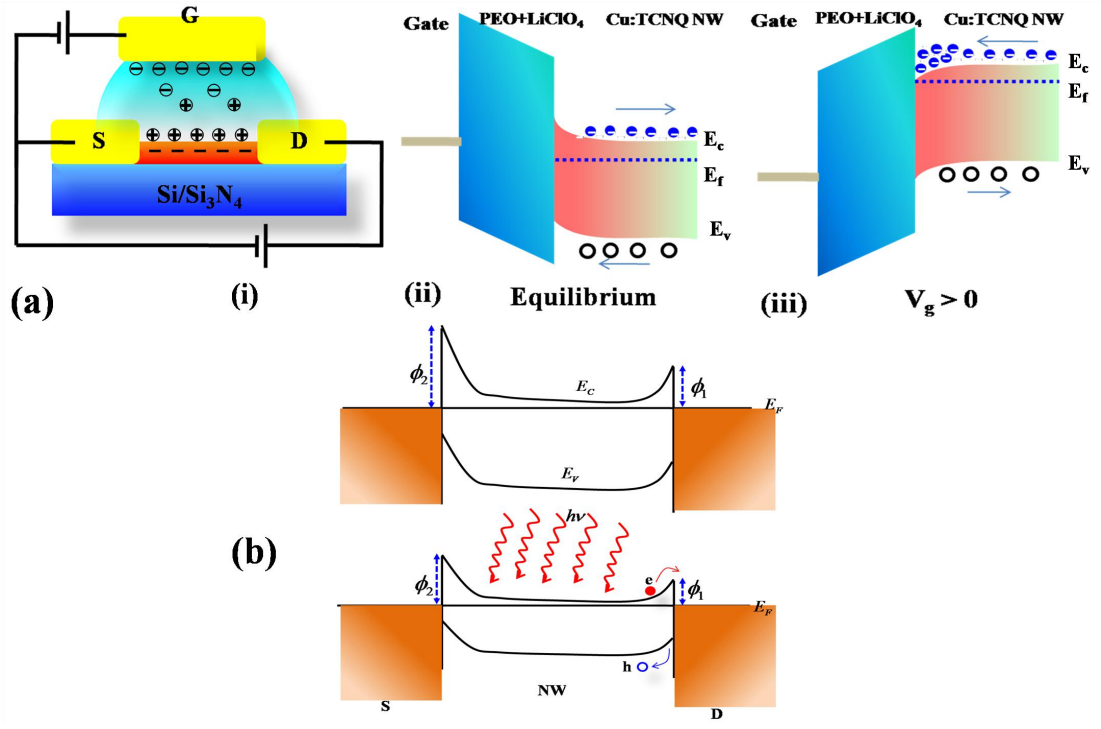

Figure 4: (A) (i) Schematic diagram of an EDLT with a Cu: TCNQ single nanowire channel. G, D, and S denote the gate, drain and source drain current, respectively. Open circles with '−' and '+'signs represent K+, ClO4−, and '−' sign represents induced electrons in the NW. (ii) and (iii) proposed model that shows how gate bias can tune the band bending on charge accumulation (B) electron-hole pair generation and barrier height reduction under illumination.

In such phototransistors, both light illumination and gate bias can be used to modulate the transport of semiconducting charge transfer complex Cu: TCNQ channels. When light is illuminated into the sample electron-hole pair is generated. These electron-hole pairs then separated and collected by the electrodes, giving rise to photocurrent. The photoconductive gain (G), that is, the number of carriers collected per photo-induced carrier, is given by the equation: $G = \frac{\tau_{life}}{\tau_{tran}} = \frac{\tau_{life}}{(L^2 / \mu . V_{DS})}$, where τ_{life} and τ_{tran} are the lifetime and carrier transit time of the photogenerated carrier, L is the channel length, μ is mobility of the channel material and V_{DS} is applied bias along the channel length. Different factors contribute to electron hole-pair separation. Existence of surface states in Cu: TCNQ NW lead to formation of depletion region near the surface that gives rise to built-in field which effectively breaks the photo generated electron-hole pair. The strong lateral field can trap the holes (for n-type conductors) thus prolonging the photogenerated carrier (here it is electron) life time (τ_{life}). Secondly, close proximity of the electrodes (~1μm in the device presented here) can reduce the carrier transit time (τ_{tran}) leading to enhancement of the photoconductive gain G and hence I_{illu} / I_{dark} . Also, illumination can reduced barrier height between two contacts with the NW as represented in Figure 4(B) that can lead to enhancement of photocurrent.

In addition of applied gate bias, through the capacitive coupling, the gate bias is expected to effectively separate the photo-generated holes and electrons, increasing their recombination time, equivalently increase lifetime τlife. Through biasing the gate terminal, our phototransistor architecture is advantageous for enhancing the photoresponse.

5. Conclusion

In summary, we have observed that applying a bias using an EDL gate to a n-channel Cu: TCNQ single NW FET, one can enhance the photoresponse of the Cu: TCNQ substantially over that which arise from the photoconductive response

alone. Synergy between the field effect induced carriers and those produced by illumination, enhances the device current which is more than the current obtained from the device when illumination and the gate act independently. The carriers created by illumination as well as gate bias enhance the device current. The effect reported here is not specific to Cu: TCNQ alone and has a generic nature that gives rise to a class of gated photodetectors

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