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Non-graded Base Si/Ge Heterojunction Transistor

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Abstract: Innovation of Heterojunction Bipolar Transistor (HBT) technology is a major game changer in wireless communication, power amplifiers and other major fields of electronics. HBTs play a vital role in extending the advantages of silicon bipolar transistors to significantly higher levels. Research on HBT is focused on reducing cost and improving reliability. These transistors have a wide range of applications namely, digital-to-analog converters, logarithmic amplifiers, RF chip sets for CDMA wireless communication systems, and power amplifiers for cellular communications. Our study focuses on utilizing the high mobility of pure Ge instead of often-used graded Ge base. Non-grtaded Ge base enhanses carrier transport which in turn increases the gain and cut-off frequency of the HBT. We have developed a high frequency, high current gain, high power gain and less noisy heterojunction bipolar transistor operating above 100GHz frequency. Lattice mismatch at emitter and collector junctions is compensated by inserting SiGe buffer layers. ATLAS TCAD - SILVACO software is used for modelling of this novel device.

Keywords: Si/Ge, Heterostructured transistor, Non-graded Ge base, Lattice matching.

1. Introduction

Heterojunction Bipolar Transistors are manufactured using variety of semiconductor materials which include Gallium Arsenide (GaAs), Silicon (Si), Gallium nitride (GaN), and Indium Phosphide (InP). The usage of commercially available transistors with a SiGe graded base is a common practice in many electronic applications[1,2]. Graded Ge base was used in design of HBT with the quantum well base[3].

Advantages of these SiGe transistors[4] over their Si counterparts are known, namely: very high operating frequency, low noise, high current gain and high power gain. The other crucial factors to be mentioned are low cost, ease of integration, mechanical stability, reduction in complexity of technology compared to other heterostructures mentioned above.

It is known that; Ge has mobility of electrons and diffusivity three times that of Si. Germanium offers an electron mobility of 3900 cm^2 $V^{-1}s^{-1}$ compared to 1280 cm^2 $V^{-1}s^{-1}$ of Silicon[5]. This significantly reduces the transit time of electrons in the base and improves the gain and operating frequency of the transistor. These transistors operate at relatively high frequencies of GHz range, and demonstrate higher emitter injection efficiencies. Even though the base is graded and not operating at its maximum possible mobility, they operate at relatively higher frequencies. In this study, we focus on using a non-graded Ge base which enhances the mobility of carriers and improves the performance of the transistor.

We used commercial package ATLAS, a technology computer aided design (TCAD) by Silvaco for our design. Recombination models were used to define mobility of carriers, as we looked to improve the device performance based on its mobility.

2. Design

2.1 Emitter and emitter-base junction

It is a well-known tendency to increase the injection of electrons from emitter to base, for it to be much larger

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than the flow of holes from base to emitter. We used heavily doped emitter and a lightly doped base. Silicon (Si) being the emitter has the following dimensions, doping and lifetime parameters as mentioned in the Table I. The area of the emitter, 1μm x 1μm is the smallest compared to other regions. We use a 0.2 μm thick Si layer as emitter. The emitter has a 1 μm long contact on the top. The intrinsic doping concentration of Si is $1.5*10^{10}$ cm^{-3}.

Emitter-Silicon	
Length	1 μm
Width	1 μm
Thickness	0.2 μm
Doping	10^{19} cm^{-3}
Lifetime of electrons	10^{-7} s
Lifetime of holes	10^{-7} s

Table 1. Modelling parameters for emitter region

The emitter is highly doped with n-type impurities in the order of $1.0*10^{19}$ cm^{-3}. We consider the most commonly used lifetime parameters for both electrons and holes in Si.

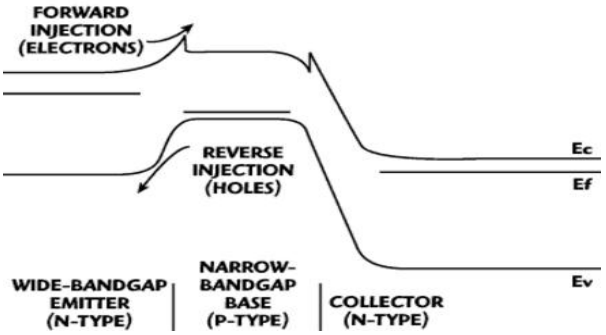

Figure 1. Band structure of n-p-n HBT design under bias with carrier flow representation

The non-graded base HBT will not allow any gradual change of energy from emitter to base. Thus, we have an abrupt junction between Emitter and Collector as seen in **Figure 1**. We have Si (Emitter) having a bandgap of 1.12 eV and Ge (Base), with a bandgap of 0.67 eV.

Due to lattice mismatch between Si and Ge, we faced structural discontinuity in the Emitter-Base junction, which impacts performance of the transistor. We designed a very thin SiGe buffer layer to reduce the lattice mismatch. The existence of buffer layer improves the injection of electrons into base.

Emitter Base Buffer Layer	
Length	1 μm
Width	1 μm
Thickness	0.0011 μm
Doping	$1.18*10^{12}$ cm^{-3}
Lifetime of electrons	10^{-8} s
Lifetime of holes	10^{-8} s

Table 2. Simulation parameters for emitter-base buffer layer

The buffer layer is 0.0011μm (1.1 nm) thick and is intrinsic in nature. $Si_{1-x}Ge_x$ buffer layer has x=0.4. The lifetime of electrons and holes, in **Table 2** are considered based on the alloy composition.

2.2 Base region

The base region stores the minority carrier charge when the transistor is in the active mode. For a n-p-n transistor, the stored electron charge in the base, Q_n, and the collector current i_c have the following relationship

$$Q_n = \tau_F i_c \quad (1)$$

where τ_F is a device constant with the dimension of time. It is called the forward base transit time and gives the average time that a charge carrier (electron) takes to cross the base.

As Equation (1) applies only for large signals, the small-signal diffusion capacitance C_{de} can be given as,

$$C_{de} = \frac{dQ_n}{dV_{BE}} = \frac{di_c}{dV_{BE}} \quad (2)$$

$$\therefore \quad C_{de} = \tau_F g_m = \tau_F \frac{I_c}{V_T} \quad (3)$$

where I_C is the dc collector bias current at which the transistor is operating.

Emitter-Base junction has an area of 0.2μm x 1μm. We use a 0.04 um (400 Angstrom) thick Ge layer as Base. The intrinsic doping concentration of Ge is 1.73e+13 cm^{-3}. The base is lightly doped with p-type impurities in the order of 4.0e+16 cm^{-3}. We consider the most commonly used lifetime parameters from **Table 3**, for both electrons and holes in Ge.

Base	
Length	2.2 μm
Width	1 μm
Thickness	0.04 μm
Doping	$4.0*10^{16}$ cm^{-3}
Lifetime of electrons	$4.0*10^{-5}$ s
Lifetime of holes	$4.0*10^{-5}$ s

Table 3. Simulation parameters for base region

The thickness of the base almost allows us to be in the quantization range (around 250-300 Angstrom). Our device shows the best performance at 400 Angstrom.

2.3 Collector and collector-base junction

Collector has the largest area out of all three regions. Larger area compensates the heat dissipated in this region due to inward flow of large number of charge carriers.

The depletion capacitance of the reverse biased Collector-Base junction is given by

$$C_\mu = \frac{C_{\mu 0}}{\left(1+\frac{V_{CB}}{V_{0c}}\right)^m} \quad (4)$$

where C_μ is the depletion capacitance; $C_{\mu 0}$ is the value of C_μ at zero voltage; V_{CB} is the magnitude of the CBJ reverse-bias voltage, V_{0c} is the CBJ built-in voltage and m is its grading coefficient.

Equations (2-4) addresses values of junction capacitances. These capacitances define cut-off frequency of the transistor.

The area of the collector, 2.2 µm x 1µm is the largest compared to other regions. We use a 0.2 µm thick Si layer as collector. The collector has a 2.2 µm long contact at the bottom. The intrinsic doping concentration of Si is 1.0e10 cm^{-3}. The emitter is moderately doped with n-type impurities in the order of 3.8e17 cm^{-3}. We consider the most commonly used lifetime parameters from Table IV, for both electrons and holes in Si.

The discontinuity can be seen at the junction formed between the base and collector like the emitter-base junction. This reduces the gain, frequency and other important performance parameters in the transistor. There is a need to match the lattice between the heterostructures. This is done by adding a buffer layer as discussed in section (II-a).

The buffer layer is 0.0011µm (1.1 nm) thick and is intrinsic in nature. $Si_{1-x}Ge_x$ has a x-composition of 0.8. Electrons from Ge base will have a smooth transition to Si if the buffer layer has parameters close to Ge, thus 80% Ge is used in the buffer. The lifetime of electrons and holes, in **Table 5**, are considered based on the alloy composition.

Collector Base Buffer Region	
Length	2.2 µm
Width	1 µm
Thickness	0.0011 µm
Doping	2.31e+13 cm^{-3}
Lifetime of electron	1.0e-08 s
Lifetime of hole	1.0e-08 s

Table 5. Simulation parameters for collector-base buffer layer

3. Simulation results

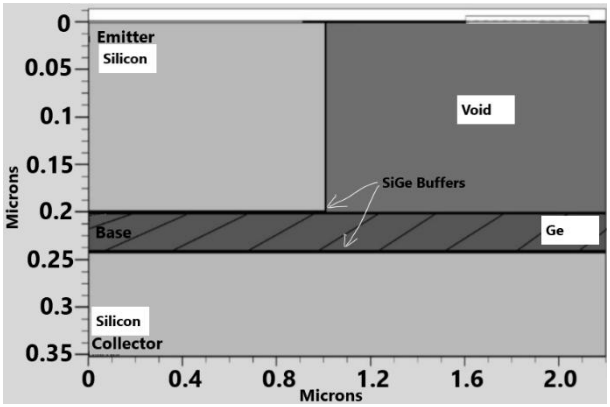

Figure 2. Structure of Non-graded base SiGe HBT

The structure in **Figure 2** shows the SiGe HBT designed under this study. This 2D plot represents the thickness of the various regions in micrometer along the length of the transistor.

The Gummel plot for our transistor with collector at 2V and various base voltages is seen in **Figure 3**. The collector current at various base currents can be observed and thus current gain factor, ß, can be computed using Gummel plot.

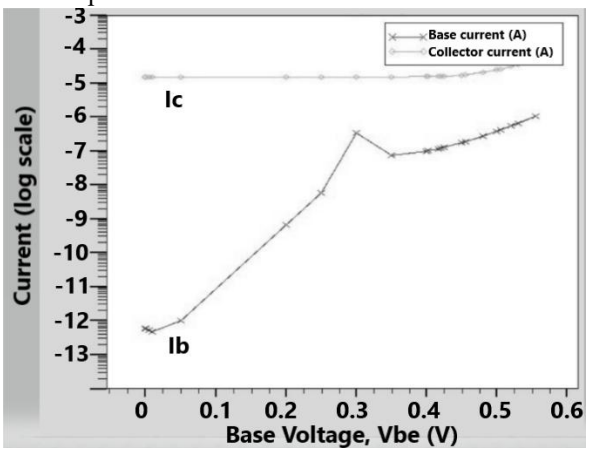

Figure 3. Gummel plot of Non-graded base SiGe HBT

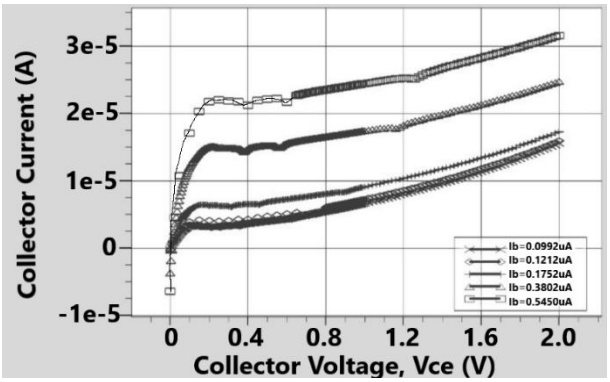

Figure 4. I-V curves for Non-graded base SiGe HBT

V_{be}	I_b	I_c
0.40 V	0.0992 µA	15.56 µA
0.42 V	0.1212 µA	15.93 µA
0.45 V	0.1752 µA	17.26 µA
0.50 V	0.3802 µA	24.78 µA
0.52 V	0.5450 µA	31.58 µA

Table 4. I_c vs V_{ce} for different I_b extracted for various V_{be}

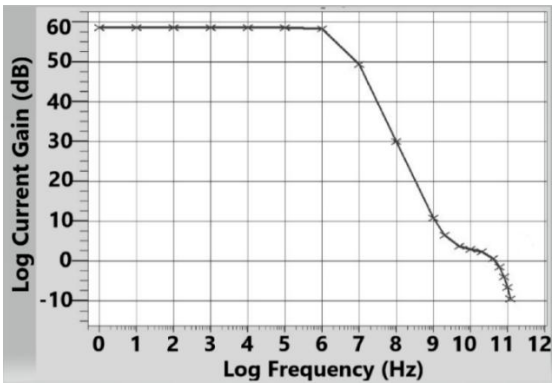

Figure 5. Current gain (dB) of Non-graded base SiGe HBT

For a transistor with common emitter configuration, the output current (I_c) is plotted against output voltage (V_{ce}) for various base biasing as seen in **Figure 4**. The values for various curves are tabulated in **Table 6**.

The AC analysis of our design is carried out by biasing the collector at 2V for various base biasing voltages. This analysis at various frequencies yields the plot in **Figure 5**. The maximum unity gain cut-off frequency, f_t, is obtained and used for the performance characteristics of HBT.

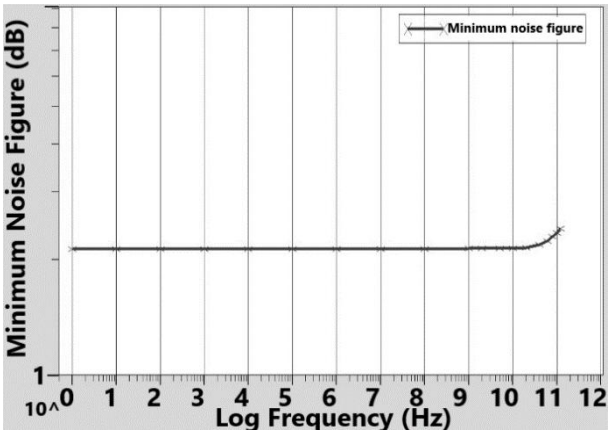

Figure 6. Minimum Noise Figure, F_{min} of Non-graded base SiGe HBT

Noise figure[7] is a figure-of-merit that describes the amount of excess noise present in a system. Minimizing the noise in the system reduces system impairments and improves the performance of the device[8]. It is one of the most important parameters for radio communications applications when assessing sensitivity. As seen in **Figure VI**, AC analysis of our device gives us the Minimum noise figure of around 2dB along the operating range of frequencies.

S21 represents the power transferred from input port to output port[9]. In general, AC analysis of the device should be done to obtain the S parameters. **Figure 7** shows the Power transfer capability of our HBT in terms of S21. The maximum oscillation frequency, f_{max} is determined by S21 vs Frequency plot

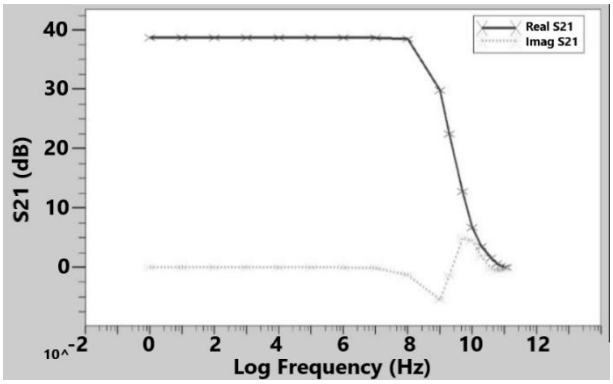

Figure VII. S21 of Non-graded base SiGe HBT

Summary of Performance of Non-graded base SiGe HBT

Table 7 summarizes the performance characteristics of our Non-graded base SiGe HBT. Section IV analyzes the performance parameters and gives a comparative study of our HBT with commercially available Graded base SiGe HBTs.

Simulation Results	
Ib (max)	0.5450 µA
Ic (max)	31.58 µA
Trans-conductance gain	34 mA/V
Current gain	59 dB
S21	15.91 dB
Minimum Noise Figure	2 dB
f_t	50 GHz
f_{max}	110 GHz

Table 7. Summary of extracted simulation results

4. Conclusion

We discussed in this study, modelling and simulation results of a non-graded base Si/Ge HBT. Ability to create heterostructure Si/Ge bipolar transistor with non-graded Ge base carries apparent mobility advantage over conventional Si BJT as well as over graded Ge base devices. Ease of integration with already existing silicon wafer technology gives Si/Ge HBTs priority in integrated design. Applications for a transistor with high gain and very high frequency of operation in addition to low noise, are many. Companies like IBM Microelectronics, Intel, and Infineon technologies, are spending billions of dollars on research on SiGe technology[10].

Looking at the research trends on SiGe technology[11], IBMs graded epi-base SiGe HBT works with the following key outputs, f_t (at V_{cb}=1V) =47GHz, f_{max} (at V_{bc}=1V) =65 GHz, Beta (β) (at V_{be}=0.72v) = 100.

A 0.5 um SiGe-HBT technology[12] with a trapezoidal Ge-profile of 8% has a f_t (at V_{cb}=1V) =32 GHz, f_{max} (at V_{bc}=1V) =45 GHz, Beta (β) (at V_{cb}=0) = 43.

Quick reference to processing steps show that the Reduced Pressure Chemical Vapor Deposition (RPCVD), high strained, Ge-graded (15.5% - 0%) SiGe film, used as a base of the HBT (Heterojunction Bipolar Transistor) developed in 0.35 µm SiGe BiCMOS process technology[13], works with DC characteristics of β = 150 and high-frequency performance, f_t = 67 GHz.

The Si/Ge heterojunction bipolar transistor process using differential epitaxy and in situ phosphorus-doped poly-Si emitter[14] at very low thermal budget is designed. A very high current gain of almost 2000 and cut-off frequency of 62 GHz were achieved for a uniform 12% Ge profile.

The Non-graded base Si/Ge HBT discussed in this paper performs well on both DC and AC parameters. A current gain of 891 (59 dB), S21 of 39 (15.91 dB), Maximum unity current gain frequency, f_t = 50 GHz and a maximum oscillation frequency of 110 GHz, was observed. A unique distinction of our device from all the comparable works is that the high frequency is associated with high gain. This improvement in almost all parameters can be credited to the pure Ge channel used in the design. Using different composition SiGe buffer layers at both junctions play an important role in achieving these results. High performance parameters coupled with easy integration with existing technology is the next step to be taken towards future electronics evolution.

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